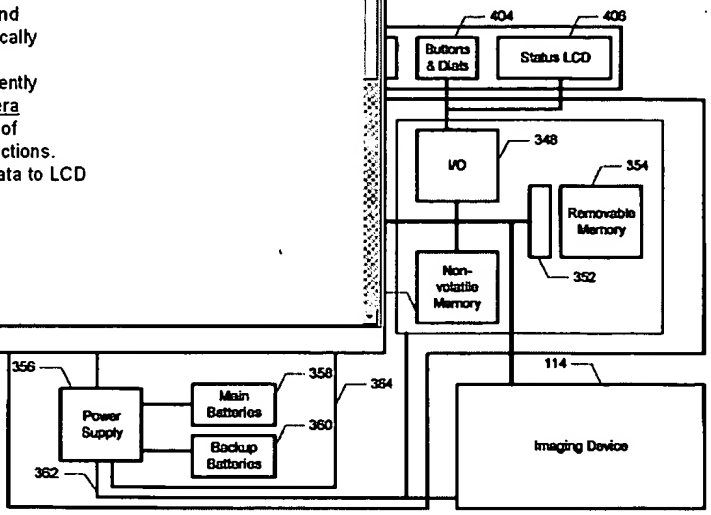
DOCUMENT-IDENTIFIER: US 6222538 B1

TITLE: Directing image capture sequences in a digital imaging device using scripts

——— KWIC ———

Detailed Description Text - DETX (8):

Power manager 342 communicates via line 366 with power supply 356 and coordinates power management operations for camera 110. CPU 344 typically includes a conventional processor device for controlling the operation of camera 110. In the preferred embodiment, CPU 344 is capable of concurrently running multiple software routines to control the various processes of camera 110 within a multithreaded environment. DRAM 346 is a contiguous block of dynamic memory which may be selectively allocated to various storage functions. LCD controller 390 accesses DRAM 346 and transfers processed image data to LCD screen 402 for display.



	U	Document ID	Issue Date	
10		US 5637871 A	19970610	Digital infrared electronic then displayed on p
11		GB 2296156 A	19960619	Digitally netwo
12		US 6222538 B1	20010424	Directing imag
13		US 6324353 B1	20011127	Document verif

US-PAT-NO: 6400471

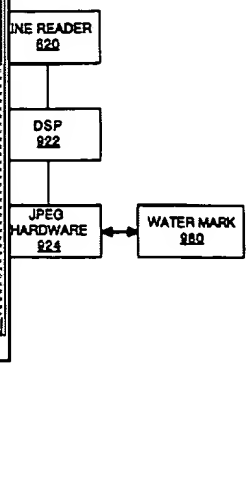
DOCUMENT-IDENTIFIER: US 6400471 B1

TITLE: Flexible architecture for image processing

——— KWIC ———

Detailed Description Text - DETX (11):
CPU 344 may include a conventional processor device for controlling the operation of digital camera 100. In the preferred embodiment, CPU 344 is capable of concurrently running multiple software routines to control the various processes of digital camera 100 within a multi-threaded environment. For example, images may be captured at the same time that previously captured images are processed in the background to effectively increase the capture rate of the camera. In a preferred embodiment, CPU 344 runs an operating system capable of providing a menu-driven graphical user interface (GUI) and software image processing. An example of such software is the Digita.TM. Operating Environment by FlashPoint Technology of San Jose, Calif.

Details | Text | Image | HTML | KWIC



	U	Document ID	Issue Date	
15	☐	US 20030158470 A1	20030821	Dual mode rea imaging and ar
16	☐	US 6678398 B2	20040113	Dual mode rea imaging and ar
17	☐	US 6400471 B1	20020604	Flexible archite
18	☑	US 6157394 A	20001205	Flexible digital image process

Details | Text | Image | HTML

Details | Text | Image | HTML | Full

Figure 9

EAST Browser - L54: (114) (multitask$3... | US 6157394 A | Tag: S.TI | Doc: 18/114 (SORTED) | Format: KWIC

File Edit View Tools Window Help

US-PAT-NO: 6157394

DOCUMENT-IDENTIFIER: US 6157394 A

TITLE: Flexible digital image processing via an image processing chain with modular image processors

——— KWIC ———

Detailed Description Text - DETX (9):

Power manager 342 communicates via line 366 with power supply 356 and coordinates power management operations for camera 110. CPU 344 typically includes a conventional processor device for controlling the operation of camera 110. In the preferred embodiment, CPU 344 is capable of concurrently running multiple software routines to control the various processes of camera 110 within a multi-threading environment. DRAM 346 is a contiguous block of dynamic memory which may be selectively allocated to various storage functions.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
16	☐	US 6678398 B2	20040113	Dual mode rea imaging and ar
17	☐	US 6400471 B1	20020604	Flexible archite
18	☐	US 6157394 A	20001205	Flexible digital image process
19	☑	US 20030210898 A1	20031113	Image recordir image reprodu information rec

Details | Text | Image | HTML

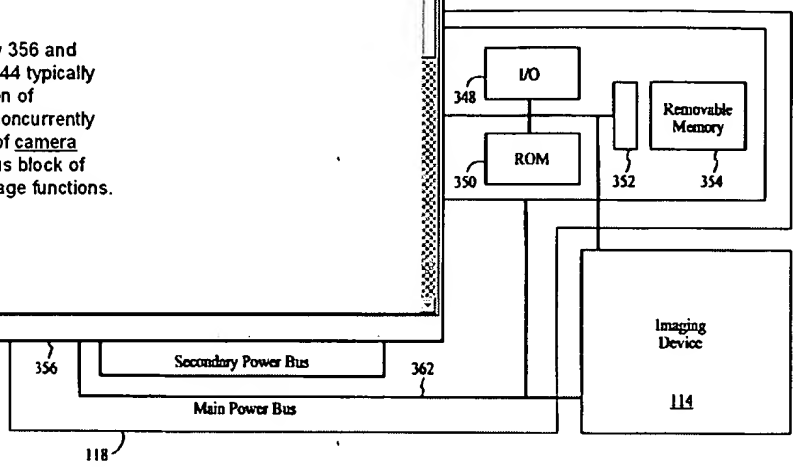


FIG. 3

Details | Text | Image | HTML | Full

DOCUMENT-IDENTIFIER: US 20020054116 A1

TITLE: Method and apparatus for editing heterogeneous media objects in a digital imaging device

——— KWIC ———

Detail Description Paragraph - DETX (7):

[0036] The CPU 124 may include a conventional microprocessor device for controlling the overall operation of camera. In the preferred embodiment, The CPU 124 is capable of concurrently running multiple software routines to control the various processes of camera within a multithreaded environment. In a preferred embodiment, The CPU 124 runs an operating system that includes a menu-driven GUI. An example of such software is the Digita.TM. Operating Environment by FlashPoint Technology of San Jose, Calif. Although the CPU 124 is preferably a microprocessor, one or more DSP 116's (digital signal processor) or ASIC's (Application Specific Integrated Circuit) could also be used.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
28	☐	US 5973734 A	19991026	Method and ap interface
29	☐	US 6587119 B1	20030701	Method and ap image during n
30	☐	US 20020054116 A1	20020509	Method and ap imaging device
31	☑	US 6317141 B1	20011113	Method and ap imaging device

Details | Text | Image | HTML

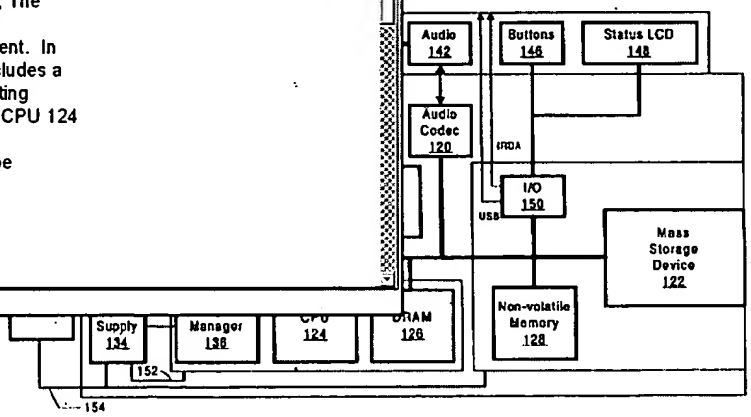


FIG. 1

Details | Text | Image | HTML | Full

In accordance with preferred embodiments, the programming is first generated as a series of instructions executable by the programmable processor device. Commercially available, "off-the-shelf" processor emulation software is used to simulate execution of the instructions in a computer. A dynamic model of electrical and mechanical portions of the disc drive is generated using commercially available, off-the-shelf plant simulation software. A dynamic linking program is configured to synchronize and transfer data between the processor emulation software and the plant simulation software. All three programs are thereafter executed simultaneously in the computer to evaluate realtime operation of the programming.

Detailed Description Text - DETX (33):

The programming is first generated as a series of instructions executable by the programmable processor device. Processor emulation software 200 is used to simulate execution of the instructions in a computer 206. A dynamic model of electrical and mechanical portions of the disc drive is generated using plant simulation software 202. A dynamic linking program 204 is configured to synchronize and transfer data between the processor emulation software and the plant simulation software. All three programs are thereafter executed simultaneously in the computer to evaluate realtime operation of the programming.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
4	☐	US 5618037 A	19970408	Method for ma
5	☐	JP 62076842 A	19870408	MULTI COMM
6	☐	US 6389384 B1	20020514	Servo process
7	☑	US 6631106 B1	20031007	Spare area wit each zone

Details | Text | Image | HTML

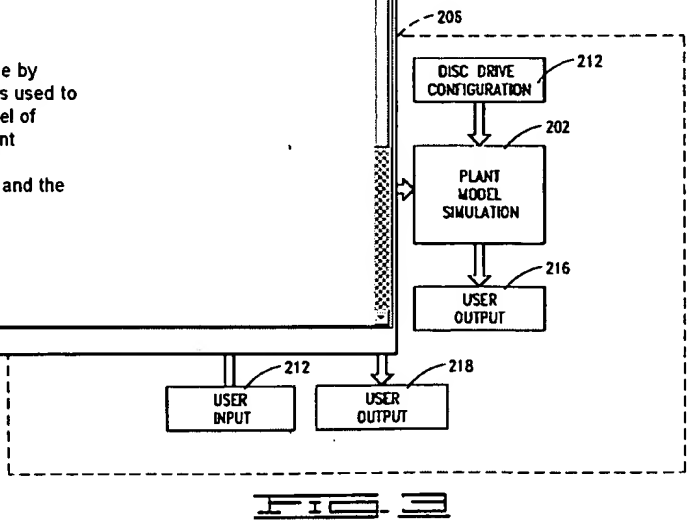


FIG. 3

Details | Text | Image | HTML | Full

EAST Browser - L54: (114) (multitask$3 ... | US 20030098914 A1 | Tag: S,P,T1 | Doc: 1/114 (SORTED) | Format : KWIC

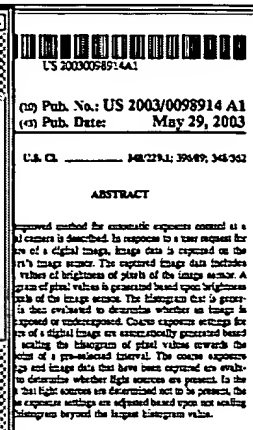
File Edit View Tools Window Help

KWIC

Detail Description Paragraph - DETX (15):

[0046] The processor (CPU) 264 typically includes a conventional processor device (e.g., microprocessor) for controlling the operation of camera 100. Implementation of the processor 264 may be accomplished in a variety of different ways. For instance, the processor 264 may be implemented as a microprocessor (e.g., MPC823 microprocessor, available from Motorola of Schaumburg, Ill.) with DSP (digital signal processing) logic blocks, memory control logic blocks, video control logic blocks, and interface logic. Alternatively, the processor 264 may be implemented as a "camera on a chip (set)" using, for instance, a Raptor II chipset (available from Conexant Systems, Inc. of Newport Beach, Calif.), a Sound Vision Clarity 2, 3, or 4 chipset (available from Sound Vision, Inc. of Wayland, Mass.), or similar chipset that integrates a processing core with image processing periphery. Processor 264 is typically capable of concurrently running multiple software routines to control the various processes of camera 100 within a multithreaded environment.

Details | Text | Image | HTML | KWIC



US 20030098914A1

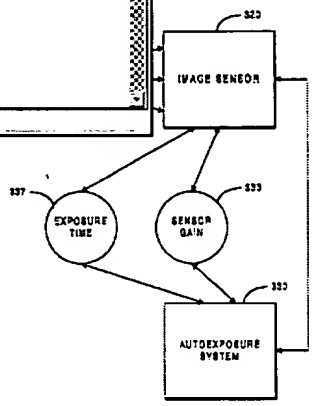
(19) Pub. No.: US 2003/0098914 A1

(43) Pub. Date: May 29, 2003

U.S. Cl. 348/229.1; 396/49; 348/362

ABSTRACT

Improved method for automatic exposure control of a digital camera is described. In response to a user request for capture of a digital image, image data is captured on the camera's image sensor. The captured image data includes digital values of brightness of pixels of the image sensor. A histogram of pixel values is generated based upon brightness levels of the image sensor. The histogram data is generated and analyzed to determine whether an image is properly exposed or underexposed. Coarse exposure settings for capture of a digital image are automatically generated based upon scaling the histogram of pixel values towards the center of a pre-selected interval. The coarse exposure settings and image data that have been captured are evaluated to determine whether light sources are present. In the event that light sources are determined not to be present, the coarse exposure settings are adjusted based upon not scaling the histogram beyond the largest histogram value.



Details | Text | Image | HTML | Full

	U	Document ID	Issue Date	
1	☐	US 20030098914 A1	20030529	Autoexposure
2	☐	US 5744322 A	19980428	Automated inci culturing device
3	☑	US 20020145403 A1	20021010	CHARGER OF FUNCTION
4	☐	US 6462508 B1	20021008	Charger of a d

Details | Text | Image | HTML

not good date

US-PAT-NO: 6157394

DOCUMENT-IDENTIFIER: US 6157394 A

TITLE: Flexible digital image processing via an processing chain with modular image proce

——— KWIC ———

Detailed Description Text - DETX (9):
Power manager 342 communicates via line 366 with po coordinates power management operations for camera 1 includes a conventional processor device for controlling th camera 110. In the preferred embodiment, CPU 344 is ca running multiple software routines to control the various p 110 within a multi-threading environment. DRAM 346 is a dynamic memory which may be selectively allocated to va

Detailed Description Text - DETX (33):
Preferably, the data pipeline required by an image proc indicated during the installation of the image processor 5

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
1	☐	US 6400471 B1	20020604	Flexible archite
2	☐	US 6157394 A	20001205	Flexible digital image process
3	☐	US 20030210898 A1	20031113	Image recordir image reprodu information rec therein, record
4	☐	US 20030033318 A1	20030213	Instantly index

Details | Text | Image | HTML

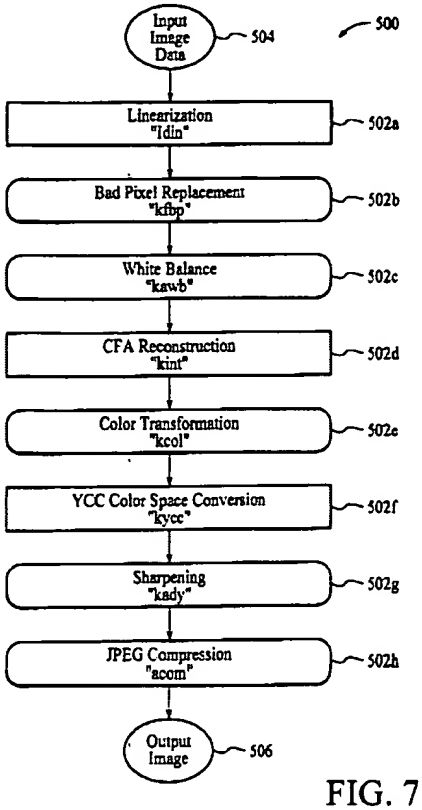


FIG. 7

Details | Text | Image | HTML | Full

EAST Browser: 150: (12) 59 and camera | US 5202992 A | Tag: S.T1 | Doc: 12/12 (SORTED) | Format: KWIC

File Edit View Tools Window Help

——— KWIC ———

Detailed Description Text - DETX (7):

When the power switch of the system is turned on, the calculation control unit 24 storing the program flow shown in FIG. 3(a) executes an initialization routine, drives the variable magnification lens component 2 and the lens component 4 for zoom compensation and focusing to the initial position specified by the signal changes of interrupters 11 and 23, and resets position memories MX and MY of the lens components 2 and 4 to a predetermined value (for example 0) when the outputs of the photo-interrupters 11 and 23 reach a predetermined signal level on account of the interruption of baffle plate 10 and 26. An AF control mode flag F.sub.M and a focusing lens control direction specification flag F.sub.D are also initialized simultaneously. Then, one of the modes indicated below is processed according to the selection status of the AUTO-MANUAL selector switch 21.

Details | Text | Image | HTML | KWIC

US005202992A

[11] Patent Number: 5,202,992

[45] Date of Patent: Apr. 13, 1993

FOREIGN PATENT DOCUMENTS

[illegible] Japan .
[illegible] Japan .
[illegible] Japan .
[illegible] Japan 359/677
[illegible] Japan 359/677
[illegible] Japan 359/671

[illegible] Examiner—Bruce Y. Arnold
[illegible] Examiner—Thong Nguyen
[illegible] Agent, or Firm—Finnegan, Henderson, [illegible], Garrett & Dunner

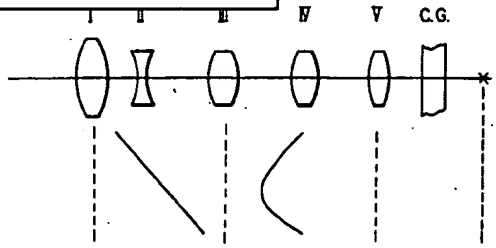
ABSTRACT

[illegible] zoom lens apparatus having a lens component [illegible] is movable for variation of image magnification, [illegible] component to compensate for the shift of focus [illegible] by the variation of the image magnification and [illegible] is movable to bring an object to be photographed [illegible] focus, and a device for driving and positioning each [illegible] lens components, there is provided a controller to [illegible] of the device. The controller has a position table [illegible] each of the lens components and a memory to store [illegible] ideal positions of the lens components. The con- [illegible] troller compares each of the actual positions of the lens [illegible] components stored in the memory with the position [illegible] based on a signal for a desired magnification so [illegible] the zoom lens can focus on a predetermined image [illegible]

9 Claims, 30 Drawing Sheets

	U	Document ID	Issue Date	
10	☐	US 4845382 A	19890704	Sampling and l component, es charge-transfe
11	☐	US 4733393 A	19880322	Test method a
12	☐	US 5202992 A	19930413	Zoom lens app

Details | Text | Image | HTML



Details | Text | Image | HTML | Full

EAST Browser : L61: (24) system near3... | JP 04031811 A | Tag: S,T1 | Doc: 10/24 (SORTED) | Format : KWIC

File Edit View Tools Window Help

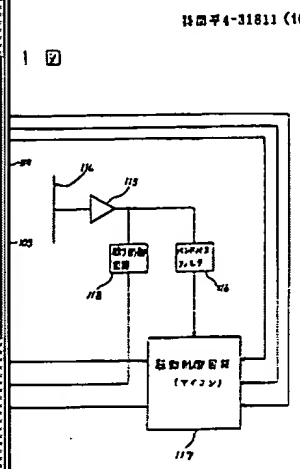
TITLE: OPTICAL CONTROLLER

——— KWIC ———

Abstract Text - FPAR (2):

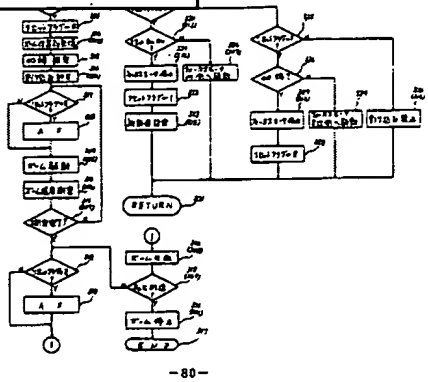
CONSTITUTION: Upon detecting that power supply is made, a drive control circuit 117 reads and stores the output value of a zoom encoder 112, namely, the position of a zoom lens 102 and processes and interrupt execution permit to the resetting program of a counter for detecting the position of a focus lens. After processing the permit, actual resetting operations is started to the counter in parallel with the speed measuring operations to a zoom lens 102. In addition, resetting operations are performed to the position counter of a focus lens 105 in accordance with the interrupt program. Thus the system initializing operations can be performed accurately in a short time, because the resetting operations can be performed simultaneously to the zoom and focus lenses in parallel with each other.

Details | Text | Image | HTML | KWIC



	U	Document ID	Issue Date	
17	☐	US 5388243 A	19950207	Multi-sort mas: deactivating its
18	☐	JP 04031811 A	19920204	OPTICAL CON
19	☐	US 20030097335 A1	20030522	Secure methoc
20	☑	US 5734820 A	19980331	Security appar

Details | Text | Image | HTML



Details | Text | Image | HTML | Full

EAST Browser: L66: (10) 63 with (ti... | US 5438190 A | Tag: S.TI | Doc: 3/10 (SORTED) | Format: KWIC

File Edit View Tools Window Help

See image for Certificate of Correction

TITLE: Lens control device

KWIC

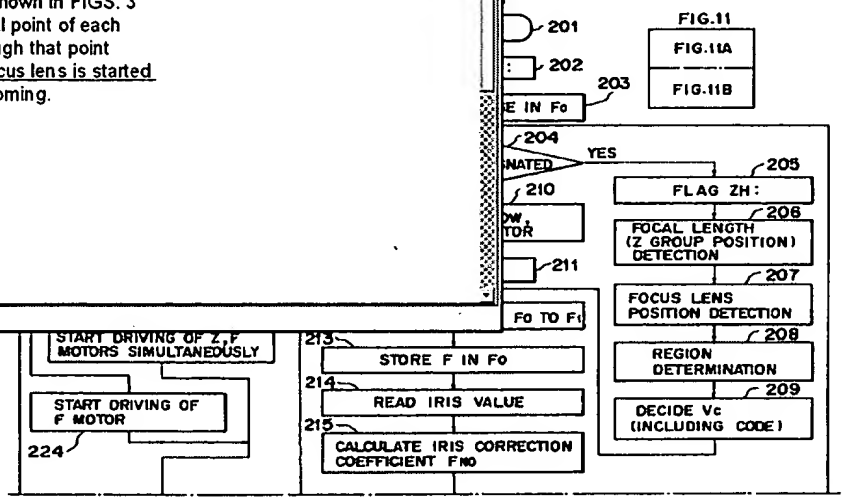
Detailed Description Text - DETX (74):

For example, in Japanese Laid-Open Patent Application No. 1-280709, a method has been disclosed in which taking the variator position in the abscissas axis and the focus lens position in the ordinate axis, the area as shown in FIGS. 3 and 5 is further subdivided into small regions, and at a central point of each region, a differential value of the focusing locus passing through that point is memorized, whereby the movement of variator lens and focus lens is started simultaneously based on the memory contents during the zooming.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
1		US 5846287 A	19981208	Consumable el
2		US 5411611 A	19950502	Consumable el
3		US 5438190 A	19950801	Lens control d
4		US 6042603 A	20000328	Method for imp

Details | Text | Image | HTML



Details | Text | Image | HTML | Full

EAST Browser - L55: (18) 54 and (init... | US 6094221 A | Tag: S | Doc: 15/18 (SORTED) | Format: KWIC

File Edit View Tools Window Help

DOCUMENT-IDENTIFIER: US 6094221 A

See image for Certificate of Correction

TITLE: System and method for using a scripting language to set digital camera device features

——— KWIC ———

Detailed Description Text - DETX (8):

CPU 344 controls camera 110 operations and may include a microprocessor device such as Motorola MPC821 manufactured by Motorola, Inc. of Schaumburg, Ill. or a Hitachi SH3 manufactured by Hitachi America, Ltd. of Terrytown, N.Y. CPU 344 optionally uses a multithreaded environment for concurrent activation of multiple camera 110 control functions. DRAM 346 is conventional DRAM selectively allocated to various storage functions including image data storage. I/O interface 348 permits host computer 120 or a user via externally-mounted user controls and an external LCD display panel to communicate with computer 118.

Detailed Description Text - DETX (19):

Function decoder 605 is a program routine for managing and decoding script messages received from control application 400. Function decoder 605 forwards

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
13	☐	US 5991465 A	19991123	Modular digital modifiable par:
14	☐	US 6154576 A	20001128	System and m·
15	☐	US 6094221 A	20000725	System and m device feature:
16	☑	US 6031964 A	20000229	System and m· digital camera

Details | Text | Image | HTML

US006094221A

[11] Patent Number: 6,094,221

[45] Date of Patent: Jul. 25, 2000

OTHER PUBLICATIONS

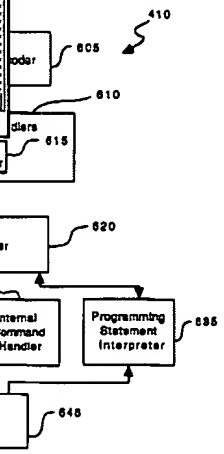
...yo Williams, Review-NEC PC-DC401 Digital Still ...era, AppleLink Newbyte, Mar. 13, 1996, pp. 1-3.

...ary Examiner—Wendy Garber
...ssor Examiner—Alicia M. Harrington
...ney, Agent, or Firm—Carr & Ferrell LLP

ABSTRACT

...stem and method for using scripts and selectable feature ...ements to configure digital camera device features. The ...al camera includes memory storing scripts for providing ...al camera device features, an interface enabling a user ...ecify feature settings, a port connectable to a host ...puter for modifying or adding scripts to the memory, ...a script manager for interpreting the scripts and the ...ure settings. The digital camera further includes an ...aging device for generating a digitized image, and image ...essors for enhancing the digitized image according to ...scripts and the selected feature settings. The digital ...era still further includes command handlers for config-...g the imaging device and the image processors accord-...to the scripts and the feature settings.

13 Claims, 12 Drawing Sheets



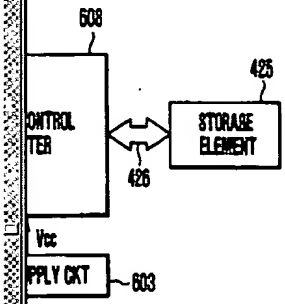
Details | Text | Image | HTML | Full

switch 601. A system control microcomputer 602 is arranged to control the whole system. A power supply circuit 603 is arranged to turn on and off the power supply in accordance with the instruction of the microcomputer 602. A transmission line 604 is arranged to transmit information on the state of the power switch 601 from the microcomputer 602 to the lens control computer 608. A transmission line 605 is provided for sending a control signal from the microcomputer 602 to the power supply circuit 603. A line 606 is provided for a power supply to the lens control computer 608. A transmission line 607 is provided for sending a power supply cutting-off signal from the lens control computer 608 to the system control microcomputer 602. When information on the off-state of the power switch 601 is sent from the microcomputer 602 to the lens control computer 608, the computer 608 allows the flow of the program to proceed from the step 503 to the step 504. After execution of the steps 504 and 505, the computer 608 sends to the system control microcomputer 602 via the transmission line 607 a signal which permits a cut-off action on the power supply. In response to this signal, the microcomputer 602 cuts off the output of the power supply circuit 603 through the transmission line 605.

(46) When the power switch 601 is turned on at the next time, the microcomputer 602 first instructs the power supply circuit 603 via the line 605 to effect the power supply to the lens control computer 608. Then, the step 509 and ensuing steps of the program are executed by the lens control computer 608.

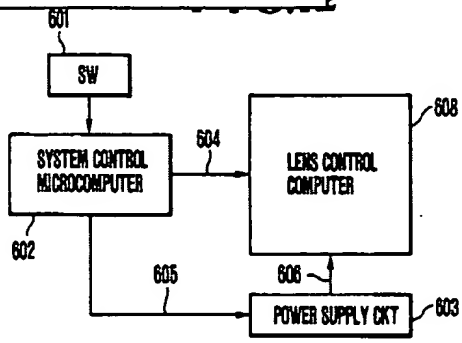
(47) Further, the element which is employed as the storage element 425 is

Details | Text | Image | HTML | FULL



	U	Document ID	Issue Date	
1	☐	US 5144491 A	19920901	Apparatus with
2	☑	US 4858012 A	19890815	Camera having
3	☑	US 5751351 A	19980512	Video camera

Details | Text | Image | HTML



Details | Text | Image | HTML | Full

Detailed Description Text - DETX (35):

Operating system utilities can include a multitask coordinator/sequencer, boot strap program to initialize the system on power up, background/foreground system crash monitor, etc. The data manager utility can include the functions of open, delete, modify, swap, sort, etc. with reference to files in memory and stored on disk. It can also perform data base management and indexing functions, as well as file management and directory keeping functions. The communications manager can provide the functions of interfacing between individual games and the master controller, providing bidirectional communications of user control, I/D, and status signals, packing and unpacking data to and from transmission, etc.

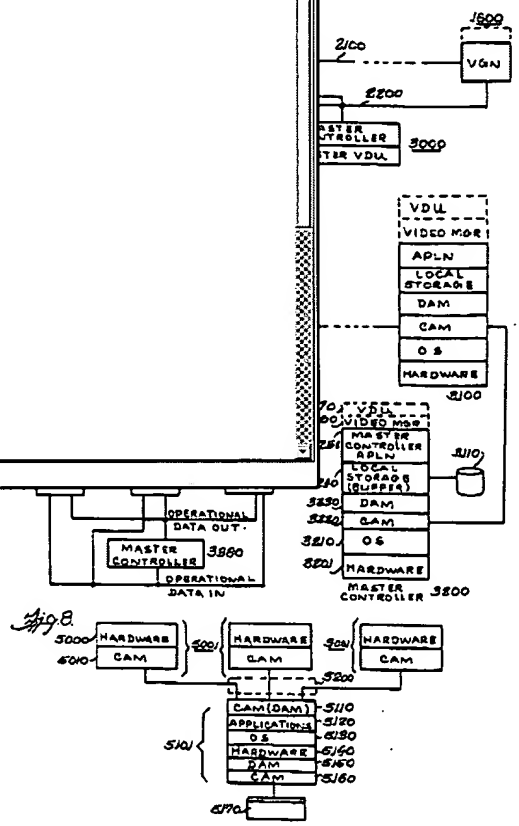
Detailed Description Text - DETX (42):

The video image input means can be comprised of numerous imaging systems. Solid state (e.g., charge couple device video sensors) or video-tube based camera imaging systems, or other technology as applicable, can be utilized in accordance with this aspect of the present invention. Various lens and focusing arrangements can be utilized, including manually or electronically (automatically) controlled focusing and exposure systems, as well as zoom, etc. features can be provided for use in conjunction with the present invention.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
15		US 5871445 A	19990216	System for ind image of the h
16		US 5851183 A	19981222	System for ind image of the h
17		US 4521014 A	19850604	Video game in
18		US 4572509 A	19860225	Video game ne

Details | Text | Image | HTML



Details | Text | Image | HTML | Full

EAST Browser - L4: (8) 1 same (simu... | JP 08286936 A | Tag: S,T1 | Doc: 7/8 (SORTED) | Format: KWIC

File Edit View Tools Window Help

DOCUMENT-IDENTIFIER: JP 08286936 A

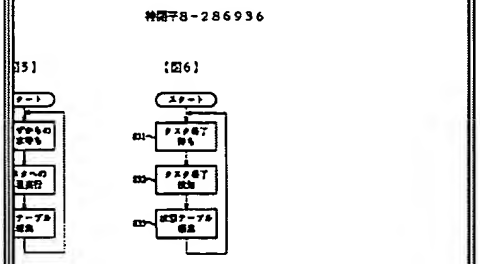
TITLE: SYSTEM STARTING DEVICE

——— KWIC ———

Abstract Text - FPAR (2):

CONSTITUTION: A multitask system is provided with a task information storage part 12 for storing the information of respective tasks, task state storage part 13 for storing the state of start/stop of each task, and initialize task 16 for reading an information table and a state table when starting the system, starting the task of 'start' and not starting the task of 'stop' based on the information table while referring to the state of start/stop of each task at the time of last system stop required for the system, after the system is started, the started task is managed and the stored contents in the task state storage part are edited (changed).

Details Text Image HTML KWIC



	U	Document ID	Issue Date	
5	☐	US 5544301 A	19960806	Object-oriente
6	☐	JP 10105415 A	19980424	REAL TIME O
7	☐	JP 08286936 A	19961101	SYSTEM STA
8	☑	JP 09146781 A	19970606	Task starting s part which sch registered into

Details Text Image HTML

Details Text Image HTML Full

Detailed Description Text - DETX (4):

Operating systems, to which the present invention applies, include those that provide for the execution of typically multiple application programs. Such operating systems typically provide general application program system services and management functions necessary to permit simultaneous execution of multiple application programs. The system services may include, but are not limited to, dynamic memory allocation of a virtual address space for use by a process within a transient program area of the main memory array 14, and basic input/output operations. Management functions include, but are not limited to the loading and initialization of applications in preparation for execution, context switch management between multiple pending processes to permit the effective simultaneous execution of multiple application programs, and support of logical communication channels for data transfer between simultaneously executing applications. The Unix.RTM. operating system, a product of AT&T, Inc., and its many variants are exemplary operating systems suitable for use with the present invention. These operating systems share the same basic architectural features including logical presentation of a disk file paradigm, a file oriented logical reference to most significant operating system services, a broad array of multiprocess management and support functions including interprocess communications such as shared memory and semaphores, as well as compatibility with a wide range of standard application programs and software development tools. In particular, LynxOS.TM., an independently implemented UNIX compatible operating system, developed and available from Lynx

Details | Text | Image | HTML | KWIC

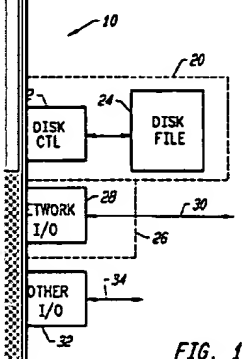


FIG. 1

	U	Document ID	Issue Date	
22	☐	US 20030160742 A1	20030828	Method for dri panel
23	☐	US 6442436 B1	20020827	Multi-tasking s recorded, and
24	☐	US 5594903 A	19970114	Operating Sys program code
25	☐	JP 04031811 A	19920204	OPTICAL CO

Details | Text | Image | HTML

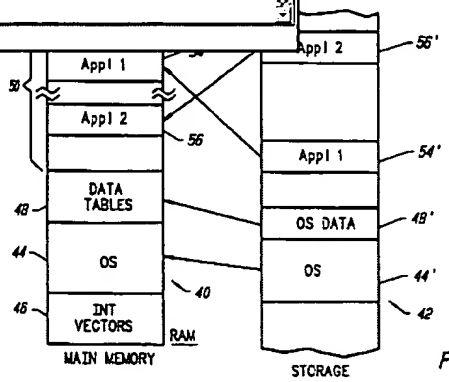


FIG. 2

Details | Text | Image | HTML | Full

US-PAT-NO: 4560889

DOCUMENT-IDENTIFIER: US 4560889 A

TITLE: Automatic clear circuit

KWIC

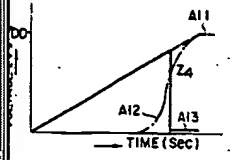
Abstract Text - ABTX (1):
In an autoclear circuit for producing reset signals for performing an initializing operation of a system simultaneously with the turning on of the system power supply, a first reset signal is produced by a delay circuit when a quickly rising power supply voltage is supplied through the input terminal connected to the power supply, and a second reset signal is produced by a Schmitt circuit when a slowly rising power supply voltage is supplied to the input terminal. Reset signals corresponding to the rise characteristics of the power supply voltage are thus produced and applied to the output terminal of the autoclear circuit to initialize the system.

Details | Text | Image | HTML | KWIC

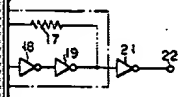
	U	Document ID	Issue Date	
1		US 4321429 A	19820323	Apparatus for :
2		US 4560889 A	19851224	Automatic clea
3		US 5220562 A	19930615	Bridge apparat bridge apparat
4		KR 2001069080 A	20010723	Channel setup

Details | Text | Image | HTML

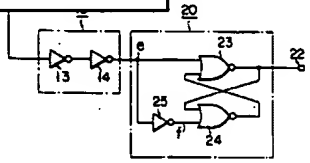
FIG. 6b



G. 7



G. 8



Details | Text | Image | HTML | Full

EAST Browser - (35) (operat$4 ne... | JP 04031811 A | Tag: S | Doc: 25/35 (SORTED) | Format : KWIC

File Edit View Tools Window Help

——— KWIC ———

Abstract Text - FPAR (2):

CONSTITUTION: Upon detecting that power supply is made, a drive control circuit 117 reads and stores the output value of a zoom encoder 112, namely, the position of a zoom lens 102 and processes and interrupt execution permit to the resetting program of a counter for detecting the position of a focus lens. After processing the permit, actual resetting operations is started to the counter in parallel with the speed measuring operations to a zoom lens 102. In addition, resetting operations are performed to the position counter of a focus lens 105 in accordance with the interrupt program. Thus the system initializing operations can be performed accurately in a short time, because the resetting operations can be performed simultaneously to the zoom and focus lenses in parallel with each other.

Document Identifier - DID (1):

JP 04031811 A

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
23	☐	US 6442436 B1	20020827	Multi-tasking s recorded, and
24	☐	US 5594903 A	19970114	Operating Syst program code
25	☐	JP 04031811 A	19920204	OPTICAL COI
26	☑	US 5960082 A	19990928	Post-initializati

Details | Text | Image | HTML

庁(JP)　⑫特許出願公開

公報(A)　平4-31811

⑬公開　平成4年(1992)2月4日

審査請求　未請求　請求項の数 3　(全12頁)

28日

区下丸子3丁目30番2号　キヤノン株式会社内

区下丸子3丁目30番2号

れていることを特徴とする光学制御装置。

(3) 特許請求の範囲第(1)項または(2)項において、

前記制御手段は前記各被制御系を定常状態の設定に応じ独立可能に構成されていることを特徴とする光学制御装置。

3. 発明の詳細な説明

(産業上の利用分野)

本発明は、光学制御装置に関し、さらに詳しくは、レンズ群の位置によって焦点を調整したり、変倍を行ったりするレンズ位置制御装置等に用いて好適なものである。

(従来の技術)

従来、カメラの動向を見ると、レンズシステムに特徴的な性能を持たせ、又、これを小型にするなどの目的から、後群レンズを移動させて焦点調整を行うレンズ、いわゆるインナーフォーカスレンズが広く用いられている。

第4図は、このインナーフォーカスタイプのレンズシステムにおけるレンズ構成の一例を示した

(1) 光学特性を変更する複数の被制御系と、

前記複数の被制御系をそれぞれ駆動する複数の駆動手段と、

前記複数の被制御系の駆動状態をそれぞれ検出する複数の検出手段と、

定常状態において、前記検出手段の検出情報に基づいて前記各駆動手段を駆動し、前記各被制御系を制御するとともに、前記定常状態となるまでの過渡状態において、前記各被制御系の初期設定動作を並行処理可能な制御手段とを備えたことを特徴とする光学制御装置。

(2) 特許請求の範囲第(1)項において、

前記光学装置は撮影動作を行うカメラであって、前記制御手段は前記初期設定動作により、撮影を開始する前に撮影中に前記各被制御系の駆動制御に関する情報を取り込むように構成さ

Details | Text | Image | HTML | Full

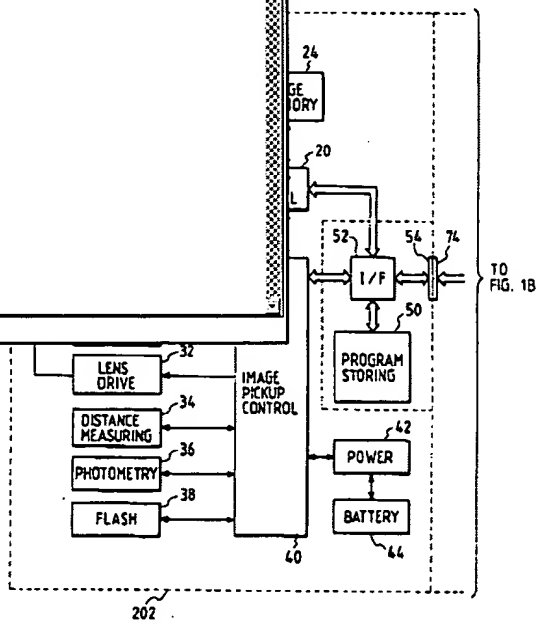
Detailed Description Text - DETX (38):
The control means 60 instructs the image pickup control circuit 40 to initialize the image pickup means 202. In response to the instruction, the image pickup control circuit 40 resets flags and variables, turns on the power circuit 42, and initializes the components in the image pickup means 202 (S23). By the initialization, the components are set to mean values, limit values, or any other values of controllable ranges.

Detailed Description Text - DETX (64):
The control means 60 in the information processing apparatus 300 instructs the image pickup control circuit 400 to initialize the image pickup means 402. In response to the instruction, the image pickup control circuit 440 resets flags and variables, turns on the power circuit 442, and initializes the components of the image pickup means (S63).

Detailed Description Text - DETX (91):
The control means 60 instructs the image pickup control circuit 540 to initialize the image pickup means 502. In response to the instruction, the image pickup control circuit 540 resets flags and variables, turns on the power circuit 542, and initializes the components of the image pickup means 502 (S83).

FIG. 1

FIG. 1A | FIG. 1B



	U	Document ID	Issue Date	
36		US 6577343 B2	20030610	Image pickup
37		US 20030043276 A1	20030306	Image process
38		US 6630949 B1	20031007	Image process
39		US 20030016378 A1	20030123	Image process

Details | Text | Image | HTML | KWIC

Details | Text | Image | HTML | Full

data. Writing a count into one of registers LRS0, LRS1 or
same count into corresponding loop count register and loc
writes the address stored in program counter PC 701 incr
the corresponding loop start address register; and writes
register LCTL 705 to enable the corresponding hardware
enable fast initialization of a multi-instruction loop. Writing
one of registers LRSE0, LRSE1 or LRSE2: writes the sam
corresponding loop count register and loop reload registe
stored in program counter PC 701 incremented in bit 3 int
loop start address register and loop end address register;
control register LCTL 705 to enable the corresponding ha
registers enable fast initialization of a loop of a single inst
registers LS0, LS1 and LS2 are loop start address registe
respectively, for corresponding hardware loops. The regi
are loop end address registers 713, 712 and 711, respect
corresponding hardware loops. Register CACHE is regist
digital image/graphics processor instruction cache coding
global temporary register 108 that stores the results of the
unit operation for later reuse upon contention or pipeline s
register is read only and an attempt to write to this registe
Registers TAG3, TAG2, TAG1 and TAG0 are cache tag r
collectively as 708, which store the relevant address porti
the data cache memory corresponding to that digital imag

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
9	☐	US 5850466 A	19981215	Golden templa
10	☐	US 5734880 A	19980331	Hardware brar status of secti
11	☐	US 5479166 A	19951226	Huffman decoc subtraction for
12	☐	US 5512896 A	19960430	Huffman encoc change for size

Details | Text | Image | HTML

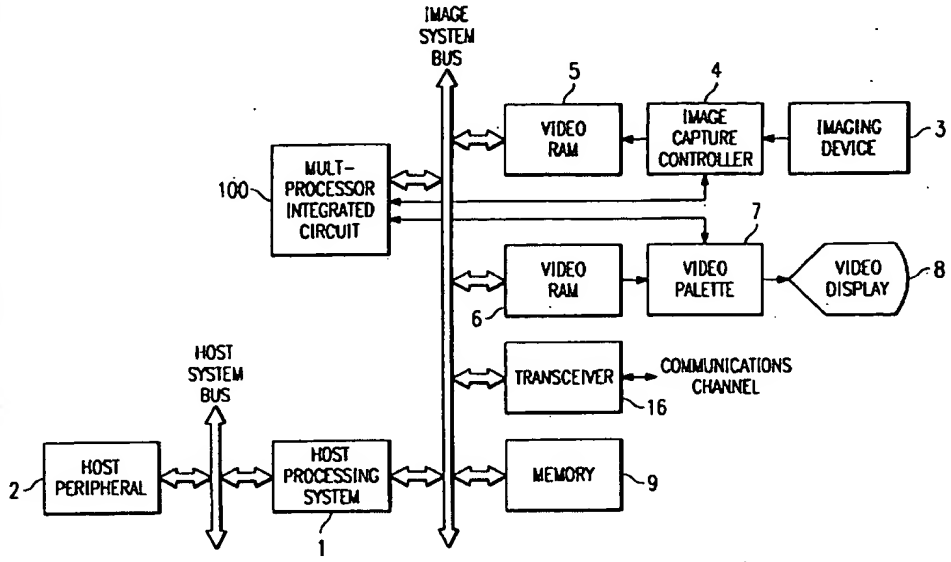


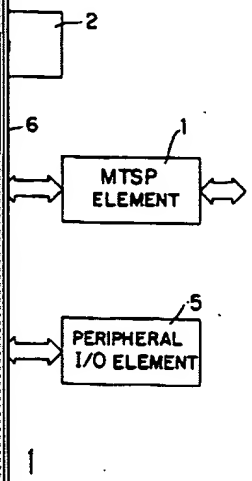
FIG. 1

Details | Text | Image | HTML | Full

a microcomputer system reflecting one of the preferred embodiments. Element (or device) 1 indicates an independent multi-task support processor for realizing the multi-task control operation embodied by the present invention. and like other peripheral devices, this element is provided as one of the I/O elements, which is hereinafter called "multi-task control element". Like any conventional microcomputer system, the multi-task control device in the preferred embodiment is also provided with the CPU 2, program memory (ROM) 3, data memory (RAM) 4, and a peripheral I/O element 5 for other I/O devices, all of which are connected to each other together with the multi-task control element 1 via bus line 6. Program memory 3 stores such programs that are independently composed of the initialized program of the multi-task control element 1 and a plurality of tasks.

Detailed Description Text - DETX (11):

As shown in FIG. 6, when the power is supplied to the system, the multi-task control element 1 first enters the reset operation to initialize all the internal functional elements (step 1). Then, the multi-task control element 1 waits, until the activated command from the CPU 2 is written into the command status register CNST (step 2). As soon as the command has been written, the multi-task control element 1 processes the command according to respective command codes (step 3). Command 0 (INIT shown in the flowchart of FIG. 7) initializes the multi-task control element 1, while this command registers the vector value to be delivered to the CPU 2 when the multi-task control element 1 generates an interrupt signal against the CPU 2, the foremost address of the



	U	Document ID	Issue Date	
8		US 6539522 B1	20030325	Method of dev system-on-chip
9		US 5018097 A	19910521	Modularly struc terminal equipr programs
10		US 5168566 A	19921201	Multi-task cont as a periphera
11		US 5063522 A	19911105	Multi-user, artr

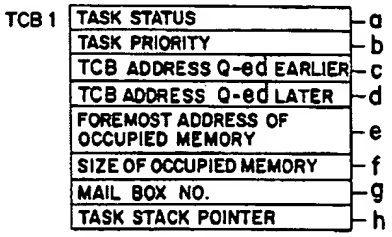


FIG. 3

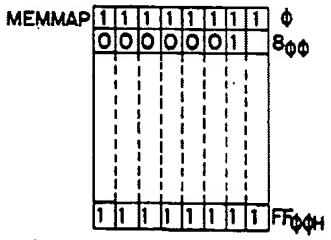


FIG. 4

a microcomputer system reflecting one of the preferred en
(or device) 1 indicates an independent multi-task support
realizing the multi-task control operation embodied by the
and like other peripheral devices, this element is provided
elements, which is hereinafter called "multi-task control el
conventional microcomputer system, the multi-task contro
preferred embodiment is also provided with the CPU 2, pr
data memory (RAM) 4, and a peripheral I/O element 5 for
of which are connected to each other together with the mu
element 1 via bus line 6. Program memory 3 stores such
independently composed of the initialized program of the
element 1 and a plurality of tasks.

Detailed Description Text - DETX (11):

As shown in FIG. 6, when the power is supplied to the s
control element 1 first enters the reset operation to initiali
internal functional elements (step 1). Then, the multi-task
waits, until the activated command from the CPU 2 is writ
status register CNST (step 2). As soon as the command
multi-task control element 1 processes the command acc
command codes (step 3). Command 0 (INIT shown in the
initializes the multi-task control element 1, while this comn
vector value to be delivered to the CPU 2 when the multi-
generates an interrupt signal against the CPU 2, the forer

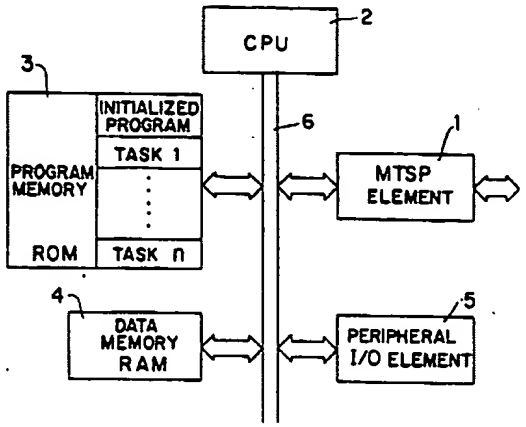


FIG. 1

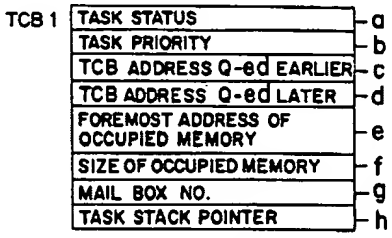


FIG. 3

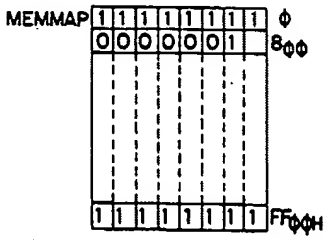


FIG. 4

Detailed Description Text - DETX (38):
The control means 60 instructs the image pickup contro
initialize the image pickup means 202. In response to the
image pickup control circuit 40 resets flags and variables,
circuit 42, and initializes the components in the image pic
By the initialization, the components are set to mean valu
any other values of controllable ranges.

Detailed Description Text - DETX (64):
The control means 60 in the information processing app
the image pickup control circuit 400 to initialize the image
In response to the instruction, the image pickup control ci
flags and variables, turns on the power circuit 442, and ini
components of the image pickup means (S63).

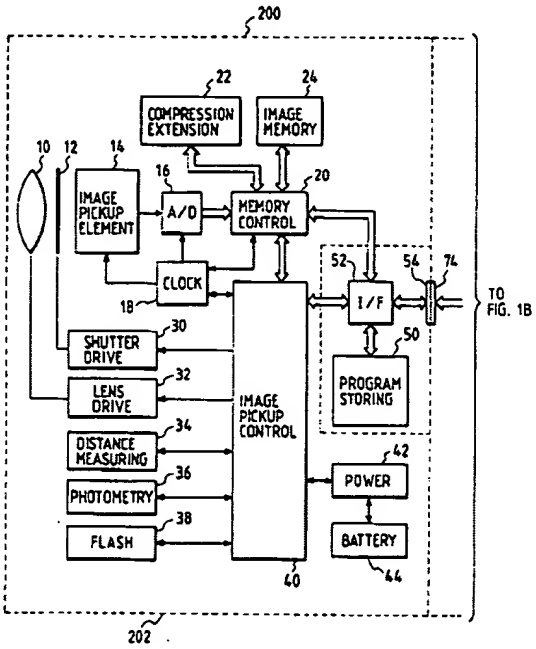
Detailed Description Text - DETX (91):
The control means 60 instructs the image pickup contro
initialize the image pickup means 502. In response to the
image pickup control circuit 540 resets flags and variables
circuit 542, and initializes the components of the image pi
(S83).

	U	Document ID	Issue Date	
36	☐	US 6577343 B2	20030610	Image pickup a
37	☐	US 20030043276 A1	20030306	Image process
38	☐	US 6630949 B1	20031007	Image process
39	☑	US 20030016378 A1	20030123	Image process

FIG. 1

FIG. 1A | FIG. 1B

FIG. 1A



main body 1 after main power is turned on. When the ma
step S1, the main body 1 always starts up in the televisio
Even if the main power of the main body 1 is turned off in
described later, by turning on the main power again, the n
up in the television mode. The television mode is a mode
television set receives ordinary television broadcasting. S
interruption by means of mode change operation, which s
another mode such as the album mode. Step S4 enables
turning off the main power. The flow is advanced to step

Detail Description Paragraph - DETX (122):

[0182] In step S10, it is determined whether the image s
standby after receiving very small current. When it is dete
image storage 4 is on standby, the flow is advanced to ste
it is instructed that the power source of the image storage
the image storage 4 starts up. In step 12, the operation th
read out completion interruption is performed. The data r
interruption is necessary for reading out data.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
17	☐	US 20020054212 A1	20020509	Digital electron through a deta
18	☐	US 5850487 A	19981215	Digital image p
19	☐	US 20030025797 A1	20030206	Digital image s
20	☐	US 6233010 B1	20010515	Electronic still digital format c

Details | Text | Image | HTML

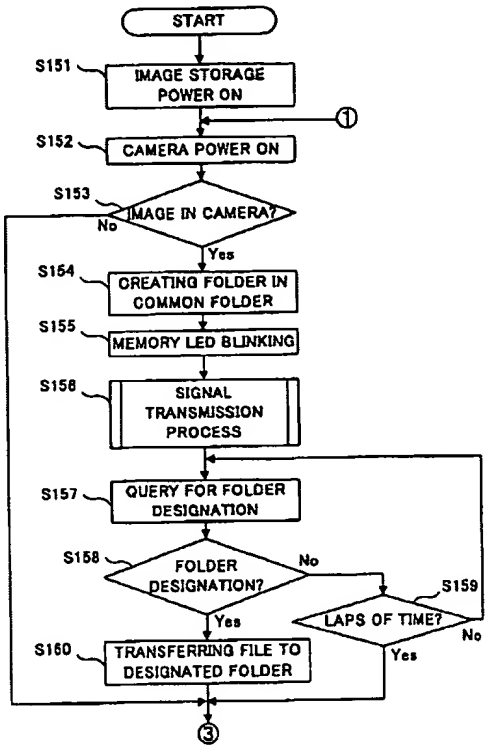


Fig 6

Details | Text | Image | HTML | Full

EAST Browser - L16: (13) 11 same (mul ... | US 5761547 A | Tag: S | Doc: 7/13 (SORTED) | Format: KWIC

File Edit View Tools Window Help

Abstract Text - ABTX (1):

An optical control system which uses multiple processors to simultaneously perform an autofocus function and an anti-vibration function. The optical control system is specifically usable in a camera lens having an optical system and which depends from a camera body having a main control unit. The optical control system, housed in the lens, is provided with a microcomputer for communication with the main control unit in the camera body, an antideflection control microcomputer, which moves the optical system so as to compensate for vibrations in the lens, and a microcomputer for ultrasonic motor drive control, which performs an autofocus function by moving the optical system with an ultrasonic motor so as to obtain a desired focus. Instructions from the main control unit in the camera body are received by the microcomputer for communication and directed, based on content, to either the antideflection control microcomputer or the microcomputer for ultrasonic motor control. In this manner, the main control unit in the camera body is freed from having to maintain two channels of communication and the microcomputers in the camera lens can operate in parallel, thus increasing the speed of processing allowing for higher quality photographs to be produced by the optical system. Further, the microcomputer for communication, based on the signals from the main control unit in the camera body, can instruct a power supply to selectively supply power to the antideflection control microcomputer and the microcomputer for ultrasonic motor control to reduce the power consumption of the lens.

Details | Text | Image | HTML | KWIC

US005761547A

Patent Number: 5,761,547

Date of Patent: Jun. 2, 1998

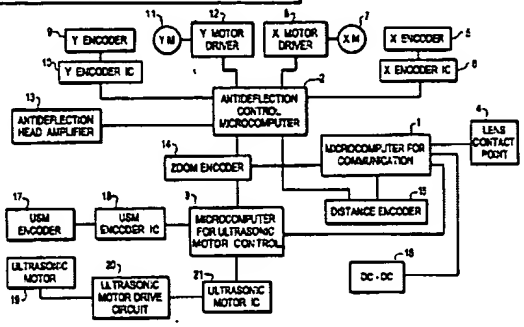
ABSTRACT

ical control system which uses multiple processors to
ssimously perform an autofocus function and an anti-
ion function. The optical control system is specifically
in a camera lens having an optical system and which
ds from a camera body having a main control unit. The
l control system, housed in the lens, is provided with
computer for communication with the main control
in the camera body, an antideflection control
computer, which moves the optical system so as to
sate for vibrations in the lens, and a microcomputer
sonic motor drive control, which performs an auto-
function by moving the optical system with an ultra-
motor so as to obtain a desired focus. Instructions from
in control unit in the camera body are received by the
computer for communication and directed, based on
t, to either the antideflection control microcomputer
microcomputer for ultrasonic motor control. In this
r, the main control unit in the camera body is freed
having to maintain two channels of communication
e microcomputers in the camera lens can operate in
l, thus increasing the speed of processing allowing for
quality photographs to be produced by the optical
. Further, the microcomputer for communication,
on the signals from the main control unit in the camera
can instruct a power supply to selectively supply
to the antideflection control microcomputer and the
computer for ultrasonic motor control to reduce the
consumption of the lens.

26 Claims, 6 Drawing Sheets

	U	Document ID	Issue Date	
5	☐	US 5142648 A	19920825	Method and ap
6	☐	US 5872594 A	19990216	Method for op movement
7	☐	US 5761547 A	19980602	Optical system
8	☑	US 5317652 A	19940531	Rotation and p

Details | Text | Image | HTML



Details | Text | Image | HTML | Full

Abstract Text - ABTX (1):

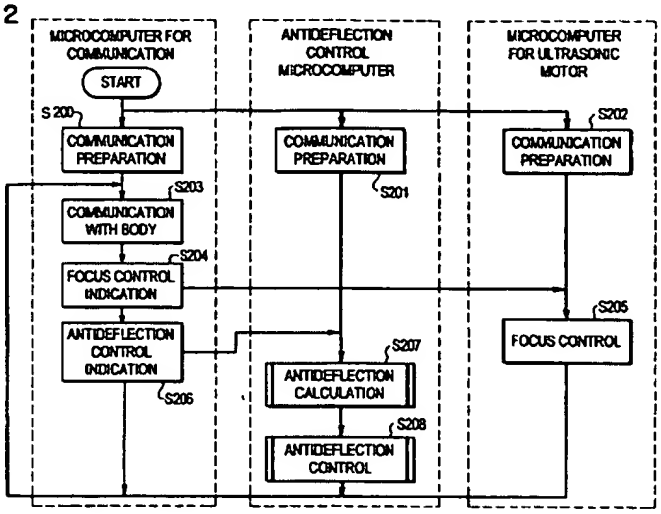
An optical control system which uses multiple processor perform an autofocus function and an anti-vibration functi control system is specifically usable in a camera lens havi and which depends from a camera body having a main co control system, housed in the lens, is provided with a micr communication with the main control unit in the camera b control microcomputer, which moves the optical system s vibrations in the lens, and a microcomputer for ultrasonic which performs an autofocus function by moving the optic ultrasonic motor so as to obtain a desired focus. Instructi control unit in the camera body are received by the microc communication and directed, based on content, to either t control microcomputer or the microcomputer for ultrasonic this manner, the main control unit in the camera body is fr maintain two channels of communication and the microco lens can operate in parallel, thus increasing the speed of for higher quality photographs to be produced by the optic the microcomputer for communication, based on the signa unit in the camera body, can instruct a power supply to se power to the antideflection control microcomputer and the ultrasonic motor control to reduce the power consumption

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
5	☐	US 5142648 A	19920825	Method and ap
6	☐	US 5872594 A	19990216	Method for op movement
7	☐	US 5761547 A	19980602	Optical system
8	☑	US 5317652 A	19940531	Rotation and p

Details | Text | Image | HTML

FIG. 2



Details | Text | Image | HTML | Full

process produces digital pro-video signals composed of plural still pictures information and which outputs the digital pro-video signals. These processes consist mainly of the operation of the video camera 1801 and the process of the video capture unit 1806, i.e. a video capture board, and thereby proceed parallel to each CPU-time-consuming process which is executed by the operating system.

Detail Description Paragraph - DETX (386):

[0591] Meanwhile, the audio capture unit 1802 is input analog audio signals from the video camera 1801, converts the signals into digital pro-audio signals by analog/digital conversion, and outputs the digital signals. The pro-audio signals are input and temporarily stacked into the audio buffering unit 1803 which rewrites the pro-audio buffer size 1804 memorized in the video and audio coding apparatus. These processes consist mainly of the operation of the video camera 1801 and the process of the audio capture unit 1802, i.e. a video capture board, and thereby proceed parallel to each process which is executed by the operating system as shown in FIG. 45. In this case, it is assumed that the process is executed parallel to the video coding process A and thereby the pro-audio buffer size reaches 30%.

Details | Text | Image | HTML | KWIC

US 20020071662A1

(19) Pub. No.: US 2002/0071662 A1
(43) Pub. Date: Jun. 13, 2002

Foreign Application Priority Data

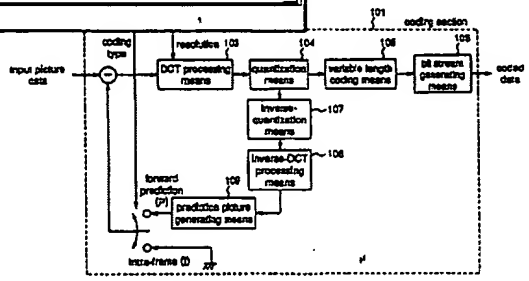
[illegible] 15, 1996 (JP) 8-272746
[illegible] 25, 1996 (JP) 8-284353
[illegible] 25, 1996 (JP) 8-314563
Feb. 25, 1997 (JP) 9-042051

Publication Classification

Int. Cl.[7] H04N 7/04
U.S. Cl. 386/109; 375/240

ABSTRACT

[illegible]ethod of coding video comprises the steps of: coding one [illegible] plurality of still picture information of pro-video [illegible]duction consisting of the plurality of still picture infor-[illegible]on is which video is digitized according to coding [illegible]meters, and deciding one or more coding parameters [illegible]d on one or more of resolution of the pro-video infor-[illegible]on, frame rate required for reproducing coded data [illegible]ting from coding, processing performance indicating [illegible]essing capability of the coding apparatus which per-[illegible]s the video coding step, and one or a plurality of coding [illegible]meters which affects amount of processing of coding in [illegible]video coding step.



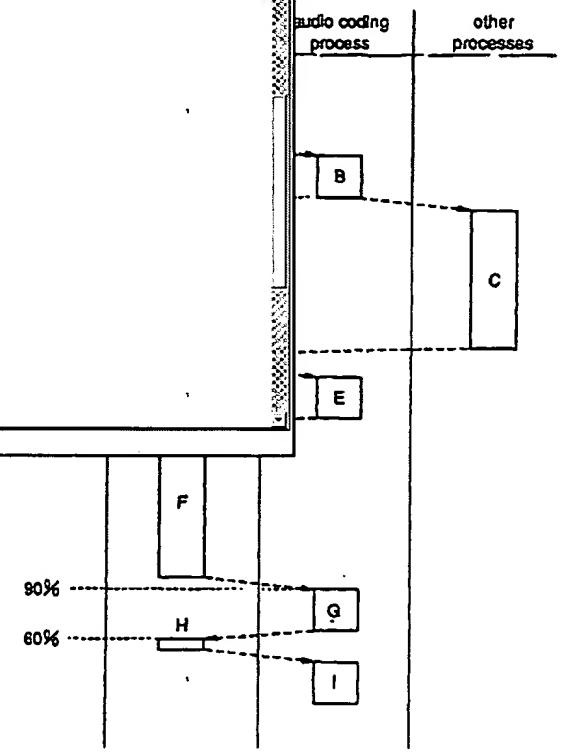
	U	Document ID	Issue Date	
1		US 20020071662 A1	20020613	Video and aud recording med
2		US 6678468 B2	20040113	Video and audi recording medi
3		US 6353703 B1	20020305	Video and audi recording medi

Details | Text | Image | HTML | Full

parallel to each CPU-time-consuming process which is executed by the operating system.

Detail Description Paragraph - DETX (386):

[0591] Meanwhile, the audio capture unit 1802 is input analog audio signals from the video camera 1801, converts the signals into digital pro-audio signals by analog/digital conversion, and outputs the digital signals. The pro-audio signals are input and temporarily stacked into the audio buffering unit 1803 which rewrites the pro-audio buffer size 1804 memorized in the video and audio coding apparatus. These processes consist mainly of the operation of the video camera 1801 and the process of the audio capture unit 1802, i.e. a video capture board, and thereby proceed parallel to each process which is executed by the operating system as shown in FIG. 45. In this case, it is assumed that the process is executed parallel to the video coding process A and thereby the pro-audio buffer size reaches 30%.



	U	Document ID	Issue Date	
1		US 20020071662 A1	20020613	Video and aud recording med
2		US 6678468 B2	20040113	Video and audi recording medi
3		US 6353703 B1	20020305	Video and audi recording medi

US-PAT-NO: 6353703

DOCUMENT-IDENTIFIER: US 6353703 B1

TITLE: Video and audio coding method, coding apparatus, and coding program recording medium

——— KWIC ———

Brief Summary Text - BSTX (85):

The audio coding apparatus constructed above is designed to input audio and perform real-time coding at a given rate. In case of general-purpose personal computer or the like, CPU processing capability is degraded by effect of another task due to multi task processing or interruption, so that audio coding cannot be performed according to initialization, which is difficult to handle.

Detailed Description Text - DETX (360):

The operation of this example of video and audio coding apparatus of the 18th embodiment is described as follows, referring to FIGS. 44 and 45. At first, the video camera 1801 captures video and audio information, and outputs separately analog video and analog audio signals. The analog video signals are

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
1	☐	US 20020071662 A1	20020613	Video and audi recording medi
2	☐	US 6678468 B2	20040113	Video and audi recording medi
3	☐	US 6353703 B1	20020305	Video and aud recording med

Details | Text | Image | HTML

US006353703B1

(10) Patent No.: US 6,353,703 B1
(45) Date of Patent: Mar. 5, 2002

WO 94/07257 3/1994
WO 95/19078 6/1996

OTHER PUBLICATIONS

...ards–Standard Video Codec Architecture for the ISA/VL...; D.J. Fairbairn; Proceedings of the International Con...ce on Signal Processing Applications and Technology; ...2, Oct. 18, 1994; pp. 1173–1178, XP000602802; p. ...h, right-hand column, line 8–line 26; p. 1178, left-hand ...mn, line 32–right-hand column, line 1; Figure 5.

...kkop Video (1) Multimedials Anwendungen im ...oberstieh"; H. Zander; Fernseh- Und Kino-Technik, ...1, 1994, pp. 303–310, XP000457151; p. 309, left-hand ...mn, line 1–line 15.

..."Tutorial on MPEG/Audio Compression"; D. Pan; IEEE ...Simedia, vol. 2, No. 2, 1995; pp. 60–74; XP000525989 ...51, right-hand column, line 1–line 13" *figures 1, 2*.

...l-Time MPEG–Audio Coding and Decoding on a DSP ...5"; C.D. Murphy et al.; IEEE Transactions on Consumer ...ronics, vol. 43, No. 1; Feb. 1997, pp. 40–47, ...00703455 *paragraph IV.A; figures 2, 5–7*.

...nforming the PC Into a TV, Radio, VCR Editing ...ol"; R. Willner; Wescon '95 Conference Record; Nov. ...995, pp. 743–748, XP000585646 *p. 744, line 6–line

(List continued on next page.)

...ary Examiner—Huy Nguyen
Attorney, Agent, or Firm—Pebbard & Wendel, L.L.P.

ABSTRACT

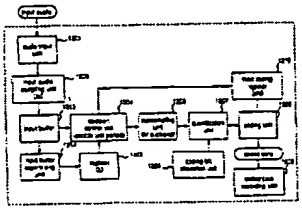
...thod of coding video comprises the steps of: coding one ...plurality of still picture information of pre-video ...rmation consisting of the plurality of still picture infor...ion in which video is digitized according to coding ...rameters, and deciding one or more coding parameters ...d on one or more of resolution of the pre-video information, frame rate required for reproducing coded data resulting from coding, processing performance indicating processing capability of the coding apparatus which performs the video coding step, and one or a plurality of coding parameters which affects amount of processing of coding in the video coding step.

34 Claims, 66 Drawing Sheets

5,335,124 A 8/1994 Keith 348/351
5,488,595 A 1/1996 Carter 359/700
5,568,274 A * 10/1996 Pejhanel et al. 358/107

FOREIGN PATENT DOCUMENTS

EP 0 597 944 A2 4/1994
JP 7-64595 3/1995
JP 2587591 12/1996



Details | Text | Image | HTML | Full

US-PAT-NO: 5036399

DOCUMENT-IDENTIFIER: US 5036399 A

TITLE: Phase controlled camera system having detachable lens

KWIC

Detailed Description Text - DETX (18):

The camera microcomputer 308 outputs CS signal in synchronization with V-sync signal supplied from the sync separation circuit 305 and simultaneously initializes (clears) a time reference counter 308' provided in the camera microcomputer 308. Count-up of this counter is continued until V-sync signal rises next. CS signal is output until the communication between the camera unit and the lens unit is completed. The lens microcomputer 206 prepares for receiving of communication data in response to the input of CS signal and simultaneously initializes (clears) an internal time reference counter 206'. Count-up of this counter is continued until CS signal or, substantially, V-sync signal rises next.

Details | Text | Image | HTML | KWIC

	U	Document ID	Issue Date	
5	☐	US 4763154 A	19880809	Focus detectin
6	☐	US 5598248 A	19970128	Optical appara
7	☐	US 5036399 A	19910730	Phase controll

Details | Text | Image | HTML

[45] Date of Patent: Jul. 30, 1991

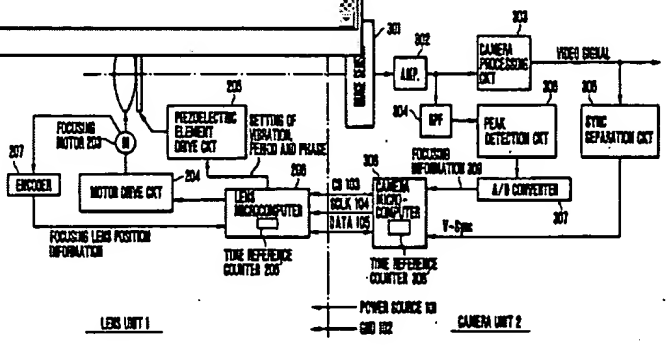
4,320,417 3/1982 Hamma et al. 358/225
4,790,649 12/1988 Harada et al. 354/286
4,872,058 10/1989 Baba et al. 354/402

Primary Examiner—James J. Groody
Assistant Examiner—Wendy R. Greening
Attorney, Agent, or Firm—Robin, Blecker, Daley & Driscoll

ABSTRACT

A camera system comprising a lens unit and a camera unit detachably attached to each other, the camera system having a control circuit for controlling the operation of the lens unit and the operation of the camera unit so as to synchronize a phase of the operation of the lens unit with a phase of operation of the camera unit, and a communication circuit for effecting communication between the camera unit and the lens unit by using a reference signal for obtaining the synchronization between the phase of operation of the lens unit and the phase of operation of the camera unit.

42 Claims, 6 Drawing Sheets



Details | Text | Image | HTML | Full

EAST Browser - L16: (13) 11 same (mul... | JP 02179628 A | Tag: S,T1 | Doc: 1/13 (SORTED) | Format: FULL

File Edit View Tools Window Help

ABSTRACT:

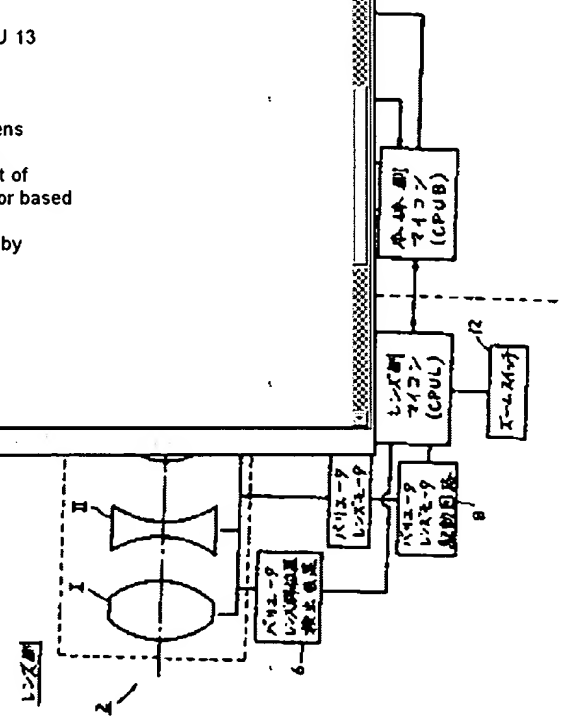
PURPOSE: To allow a camera side and a lens side to independently process data in parallel and to operate the shifting amount of a focusing lens only when necessary by providing CPUs on the camera main body side and the lens side.

CONSTITUTION: When a zoom switch 12 is depressed, the lens side CPU 13 transmits a signal to a variator lens motor driving circuit 8, drives a variator lens motor 7 and shifts a variator lens group 3 in tele direction or wide direction. When the focal distance changes with the shift, a variator lens group position detecting device 6 detects the change and informs the lens side CPU 13 of the change. The lens side CPU 13 operates the focal point correcting amount at the present focal point position and outputs the amount of the main body side CPU 14. The main body side CPU 14 drives an AF motor based on the signal and carries out the position adjustment of the focusing lens group 4. Focus control is performed while driving the focusing lens group 4 by the main body side CPU 14.

Details | Text | Image | HTML | FULL

	U	Document ID	Issue Date	
1	☐	JP 02179628 A	19900712	CAMERA PRC
2	☐	US 4205780 A	19800603	Document proc
3	☐	JP 06222012 A	19940812	IMAGE PROC INSPECTION :
4	☐	US 5168365 A	19921201	Interchangeabl

Details | Text | Image | HTML

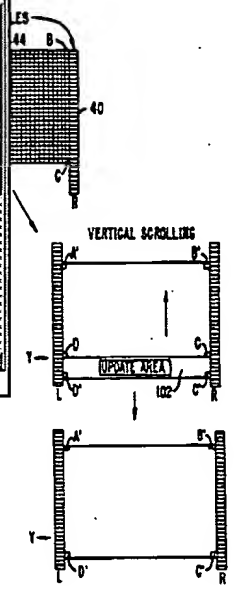


Details | Text | Image | HTML | Clipped

to represent an image. Compression involves passing the raw image data into a compressor, which combines and analyzes the patterns in the raw data to produce a compressed image file where the original image is not readily discernable without a corresponding decompression.

Detailed Description Text - DETX (11):

During initialization, block decoder 24 operates in parallel with edge value calculator 26, although in other embodiments, their operation is serial or totally independent. Edge value calculator 26 scans the MCUs in compressed image memory 12, evaluating only the differential values in each MCU, which being differential, require reference to a reference MCU. For one standard, the JPEG standard, each MCU contains a differential value for DC intensity, and the reference MCU for any MCU is the MCU for the block to the left of the block being decoded. For example, to find the absolute DC value for block n+2 (see FIG. 2), a differential value is extracted from MCU n+2 and the absolute DC value for block n+1 is subtracted from the extracted value. However, since block n+1 is not decompressed, (since it is not within virtual image 44), only the DC value is extracted from that block by edge value calculator 26. To avoid the delays when panning a virtual image across a full image, left and right edge tables 38,40 are provided.



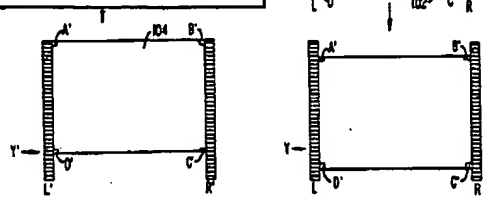


FIG. 4

	U	Document ID	Issue Date	
4		US 5633995 A	19970527	Camera syster
5		US 5408328 A	19950418	Compressed ir
6		US 5327248 A	19940705	Compressed ir
7		JP 11194847 A	19990721	Computer syst equipment e.g. circuit which se